REMARKS

The above amendments are made in response to the Office Action mailed August 6, 2007. Claims 1-20 are pending in the present application and stand rejected. The Examiner's reconsideration is respectfully requested in view of the following remarks.

Claim Rejections - § 102

1) Claims 1, 13, and 14 stand rejected under 35 U.S.C 102(e) as being anticipated by Sheffer [U.S. Patent No. 6,543,041], as set forth in paragraph 1 of the Office Action.

It is respectfully submitted that Sheffer does not disclose or suggest the limitation of "*using the structural metric during the logical synthesis to predict wiring congestion of the circuit design model to optimize the circuit design model*", as essentially recited in claims 1, 13, and 14.

The Examiner contends that Sheffer discloses the above limitation in FIG. 1, FIG. 3 and col. 3, lines 62-64. Applicants respectfully disagree because Sheffer does not consider wiring congestion during logical synthesis. In fact, any consideration of wiring congestion by Sheffer is performed after logical synthesis. Sheffer states (in col. 3, lines 58-60 and lines 62-64) that "step 304 tentatively routes the connections for the gates in the netlist by using either Steiner tree routing or global routing" and "[g]lobal routing is an interconnection pattern that does consider the congestion caused by the other routes." However, Sheffer discloses (in col. 3, lines 31-41 and 54-57) that step 304 is performed in the placing process 112, which is clearly performed after the step of logical synthesis 108 in FIG. 1.

Further, as described in paragraph 7 of Applicants U.S. Patent Publication 2005/0183046, design closure includes the steps of logical synthesis followed by physical

design and "[p]hysical design takes the circuits and assigns them physical locations". Accordingly, claims 1, 13, and 14 have been amended for the purpose of clarifying that the claimed steps of logical synthesis occur before assigning physical locations to circuits. This means that the claimed inventions consider wiring congestion before assigning physical locations to circuits. Any consideration of wiring congestion by Sheffer is performed after assigning physical locations to circuits. For example, step 304 of Sheffer is performed as part of step 206, which is performed after the tentative assignment or placement of each of the gates in the gate level netlist onto physical locations on a chip floor (See col. 3, lines 36-38 and FIG. 2).

For at least the foregoing reasons, Sheffer fails to anticipate claims 1, 13, and 14. Thus, claims 1, 13 and 14 are believed to be patentable over Sheffer. Moreover, claims 2-12 and claims 15-20 are believed to be patentable over Sheffer at least by virtue of their respective dependencies from claims 1 and 14.

2) Claims 1, 13, and 14 stand rejected under 35 U.S.C 102(e) as being anticipated by Weaver [U.S. Patent Pub. 2004/0230933], as set forth in paragraph 2 of the Office Action.

It is respectfully submitted that Weaver does not disclose or suggest the limitation of "*determining a structural metric through an analysis of the logic network, wherein the structural metric is a measure of wiring congestion of the circuit design model*", as essentially recited in claims 1, 13, and 14.

The Examiner contends that Weaver discloses the above limitation in block 2 and paragraph 15. Applicants respectfully disagree. Block 2 (step 2) and paragraph 15 merely disclose a design synthesis stage. However, there is no mention in the cited paragraph nor

elsewhere in Weaver of the design synthesis stage determining a structural metric from a logic network that is a measure of wiring congestion. In fact, wiring congestion is not mentioned in Weaver until block 8 (or step 8). Paragraph 34 of Weaver teaches that during step 8, congestion is considered after placement of the cells. However, the claimed step of determining a structural metric is performed during logical synthesis, which is before placement. As discussed above, claims 1, 13, and 14 were amended to clarify that the claimed steps of logical synthesis occur before assigning physical locations to circuits.

For at least the foregoing reasons, Weaver fails to anticipate claims 1, 13, and 14. Thus, claims 1, 13 and 14 are believed to be patentable over Weaver. Moreover, claims 2-12 and claims 15-20 are at least believed to be patentable over Weaver by virtue of their respective dependencies from claims 1 and 14.

3) Claims 1-20 stand rejected under 35 U.S.C 102(e) as being anticipated by McElvain [U.S. Patent Pub. 2006/0095872], as set forth in paragraph 3 of the Office Action.

It is respectfully submitted that McElvain does not disclose or suggest the limitation of "*generating a logic network from the RTL textual description of the circuit design model* and *determining a structural metric through an analysis of the logic network, wherein the structural metric is a measure of wiring congestion of the circuit design model*", as essentially recited in claims 1, 13, and 14.

The Examiner contends that McElvain discloses or suggest the above limitation in figures 22, 35 and paragraphs 111 and 126. Applicants respectfully disagree because McElvain does not consider congestion until after logic synthesis. While paragraph 123 discloses that operation 1001 of FIG. 22 performs logic synthesis to create a logic element

network, there is no disclosure in McElvain of *determining a structural metric (*during logical synthesis*) through an analysis of the logic network, wherein the structural metric is a measure of wiring congestion of the circuit design model.* Further FIG. 22 shows that optimization 1005 takes place after logic synthesis 1001. Paragraphs 111 and 116 teach analyzing congestion by taking into account the presence of a shielding mesh. However, such analysis, as shown as step 1005 in FIG. 22, is performed after logical synthesis, and the claimed determining of the structural metric is performed during logic synthesis. McElvain also performs its optimization 1005 after placement of the circuits, which is different from the amended claims, which recite the determining of the structural metric being performed before placement of the circuits. While element 1450 of figure 35 shows production of a congestion estimate, as written in element 1450, the estimation is performed after the placement of the circuits, which is different from the amended claims.

For at least the foregoing reasons, McElvain fails to anticipate claims 1, 13, and 14. Thus, claims 1, 13 and 14 are believed to be patentable over McElvain. Moreover, claims 2-12 and claims 15-20 are at least believed to be patentable over McElvain by virtue of their respective dependencies from claims 1 and 14.

Conclusion

In view of the foregoing remarks, it is respectfully submitted that all the claims now pending in the application are in condition for allowance. Early and favorable reconsideration is respectfully requested.

Respectfully submitted,

By: Robert J Newman

Robert J. Newman
Reg. No. 60,718
Attorney for Applicants

F. CHAU & ASSOCIATES, LLC
130 Woodbury Road
Woodbury, NY 11797
Telephone: (516) 692-8888
Facsimile: (516) 692-8889